First Named Inventor	Frankie F. Roohparvar
Serial No.	10/798,065
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Group Art Unit	2186
Examiner Name	Behzad Peikari
Confirmation No.	5675
Attorney Docket No.	400.044US02

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Title: Synchronous Flash Memory with Accessible Page During Write

Total Pages: 8 (including transmittal sheet)

Commissioner for Patents
Attention: EXAMINER BEHZAD PEIKARI
P. O. Box 1450
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Enclosures

The following documents are attached:
X A Proposed Amendment to the claims (7 pages).

MESSAGE: In further to the phone conversation between attorney Andrew Walseth and Examiner Peikari, attached are Proposed Amendments to the claims. If the Examiner has any further questions or concerns, please feel free to contact the attorney Walseth at direct dial (612) 312-2207.

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Submitted By

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Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to the United States Patent and Trademark Office on December 8, 2004.

Name	Andrew C. Walseth (Attorney) Reg. No. 43,234	Signature	

First Named Inventor	Frankie F. Roohparvar	**PROPOSED AMENDMENT TO THE CLAIMS**
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Filing Date	March 11, 2004	
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Please amend the claims as follows:

1. (original) A method of operating a flash memory comprising:
copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory;
performing a write operation to write second data to the first array bank in response to an external processor coupled to the flash memory;
reading the first data from the buffer circuit using the external processor while performing the write operation, wherein the first data contains instruction code for the processor; and
monitoring the write operation with the external processor in response to the instruction code.

2. (original) The method of claim 1, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.

3. (original) The method of claim 1, further comprises reading third data from a second array bank with a second external processor while performing the write operation.

4. (original) The method of claim 1, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.

5. (original) The method of claim 1, wherein copying first data to the buffer circuit is performed in response to an externally provided command from the external processor.

6. (original) A method of operating a flash memory comprising:
copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to a command from an external processor coupled to the flash memory;
performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;
reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the processor, wherein the first data contains instruction code for the external processor; and
monitoring a status register of the flash memory with the external processor in response to the instruction code.

7. (original) The method of claim 6, further comprises reading third data from a second array bank with a second external processor while performing the write operation.

8. (original) The method of claim 6, wherein copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to a command from an external processor coupled to the flash

memory further comprises copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to an externally provided write command from an external processor coupled to the flash memory.

9. (original) A method of operating a flash memory comprising:
receiving a write command at the flash memory, wherein the write command is provided by an external processor coupled to the flash memory;
automatically copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to the write command;
performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;
reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the external processor, wherein the first data contains instruction code for the external processor; and
monitoring a status register of the flash memory with the external processor in response to the instruction code.

10. (original) The method of claim 9, further comprises reading third data from a second array bank with a second external processor while performing the write operation.

11. (Currently Amended) A method of operating a synchronous flash memory comprising:
storing instruction code in each of a plurality of array blocks of the synchronous flash memory; [[and]]

copying the instruction code from a first array block to a buffer circuit using control circuitry of the memory, during a write operation, to the first array block using an external processor coupled to the memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation; and

monitoring the write operation with the external processor in response to the instruction code.

12. (original) The method of claim 11, wherein the synchronous flash memory comprises four array blocks.

13. (original) The method of claim 11, wherein copying the instruction code is performed in response to an externally provided write command.

14. (Currently Amended) A method of operating a flash memory comprising:

copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory;

performing a write operation to write second data to the first array bank in response to an external processor coupled to the flash memory; [[and]]

reading the first data from the buffer circuit using the external processor while performing the write operation, wherein the first data contains instruction code for the processor; and

monitoring the write operation with the external processor in response to the instruction code.

15. (Cancelled)

16. (Currently Amended) The method of ~~claim 15~~ claim 14, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.

PROPOSED AMENDMENT

17. (original) The method of claim 14, further comprises reading third data from a second array bank with a second external processor while performing the write operation.

18. (original) The method of claim 14, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.

19. (original) The method of claim 14, wherein copying first data to the buffer circuit is performed in response to an externally provided command from the external processor.

20. (Currently Amended) A method of operating a flash memory comprising:
copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to an external command;
performing a write operation to write second data to the first array bank; [[and]]
reading the first data from the buffer circuit while performing the write operation; and
monitoring the write operation with an external processor in response to instruction code.

21. (Currently Amended) The method of claim 20, wherein performing a write operation to write second data to the first array bank further comprises performing a write operation to write second data to the first array bank in response ~~to an~~ to the external processor coupled to the flash memory.

22. (original) The method of claim 21, wherein reading the first data from the buffer circuit while performing the write operation further comprises reading the first

data from the buffer circuit while performing the write operation, wherein the first data contains instruction code for the processor.

23. (original) The method of claim 22, further comprising monitoring the write operation with the external processor in response to the instruction code.

24. (original) The method of claim 23, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.

25. (original) The method of claim 20, further comprises reading third data from a second array bank while performing the write operation.

26. (original) The method of claim 25, wherein reading third data from a second array bank while performing the write operation further comprises reading third data from a second array bank with a second external processor while performing the write operation.

27. (original) The method of claim 20, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.

28. (original) The method of claim 20, wherein copying first data to the buffer circuit is performed in response to an externally provided command from an external processor.

CONCLUSION

In view of the above proposed amendments to the claims, Applicant respectfully submits that the claims would be in condition for allowance if the amendments were entered and requests reconsideration of the application and indication of allowability of the proposed amended claims.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 12/9/04

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